

150V N-Channel Power SpeedFET
• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

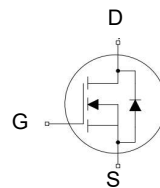
- BLDC Motor driver
- DC-DC
- Load Switch

• Ordering Information:

Part NO.	ZMSA040N15HR
Marking	ZMS040N15H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2000

• Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

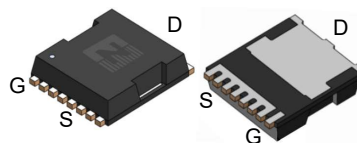
Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		150	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	180	A
	I_D	$T_C=75^\circ\text{C}$	147	A
	I_D	$T_C=100^\circ\text{C}$	127	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	720	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	300	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.8	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	756	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	1210	mJ
ESD Level (HBM)	CLASS 2			

• Product Summary


$$V_{DS} = 150\text{V}$$

$$R_{DS(ON)} = 4.2\text{m}\Omega$$

$$I_D = 180\text{A}$$



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•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.5	°C/W
Thermal resistance, junction-ambient	$R_{thJA}^{②}$		-	40	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	150			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2	3	4	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=150V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$		4.2	5.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=10A$		30		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=20A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	6008	-	pF
Output capacitance	C_{oss}		-	4614	-	
Reverse transfer capacitance	C_{rss}		-	270	-	
Gate Resistance	R_g	$f=1MHz$	-	1.8		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	88.5	-	nC
Gate - Source charge	Q_{gs}		-	24.5	-	
Gate - Drain charge	Q_{gd}		-	18	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	14.5	-	ns
Turn-ON Rise time	t_r		-	4.3	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	18.4	-	ns
Turn-Off Fall time	t_f		-	5.2	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=50A$	-	45	-	ns
Reverse Recovery Charge	Q_{RR}		-	56	-	nC



Fig.1 Gate-Charge Characteristics

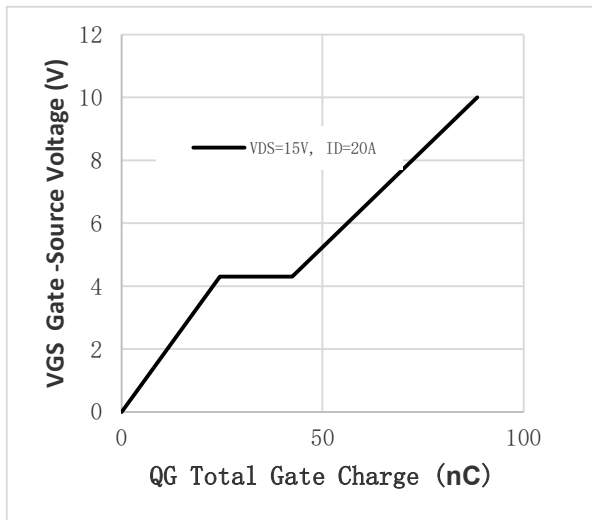


Fig.2 Capacitance Characteristics

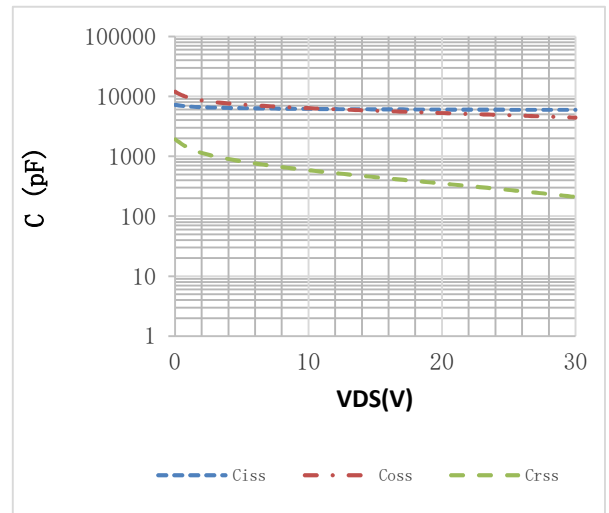


Fig.3 Power Dissipation

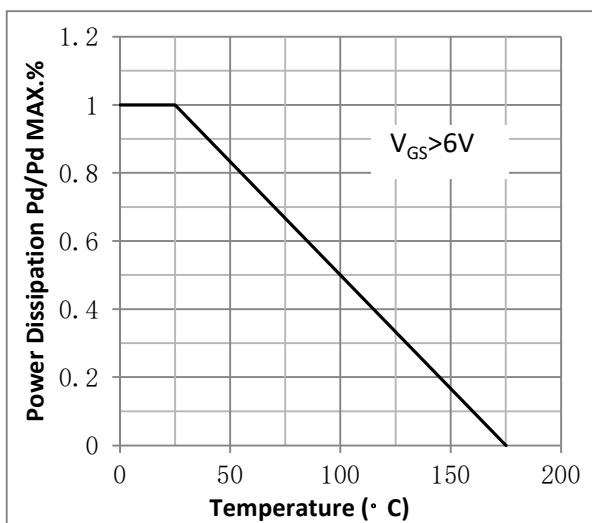


Fig.4 Typical output Characteristics

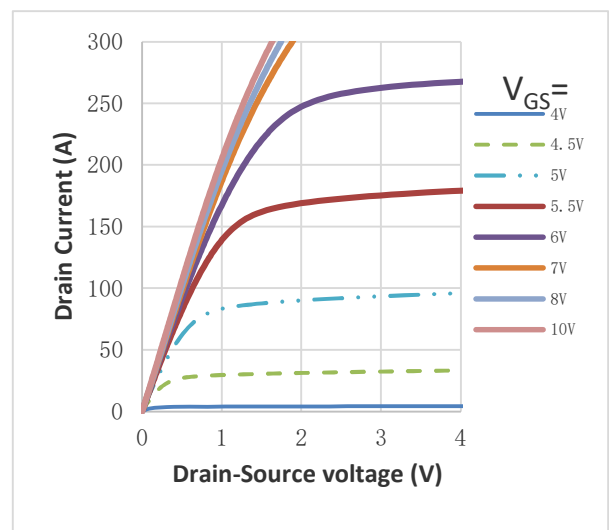


Fig.5 Threshold Voltage V.S Junction Temperature

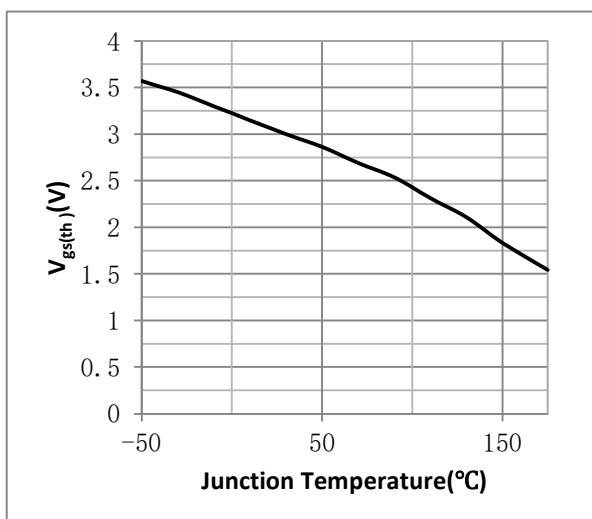


Fig.6 Resistance V.S Drain Current

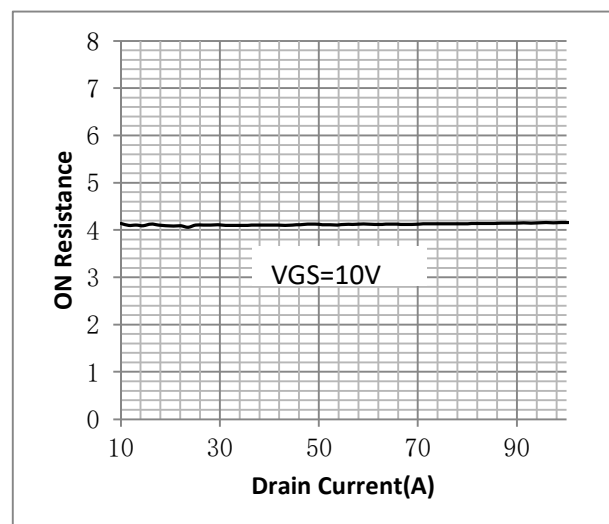




Fig.7 On-Resistance VS Gate Source Voltage

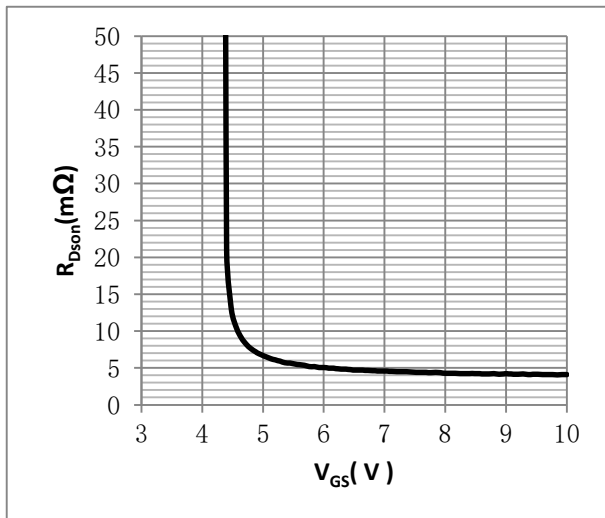


Fig.8 On-Resistance V.S Junction Temperature

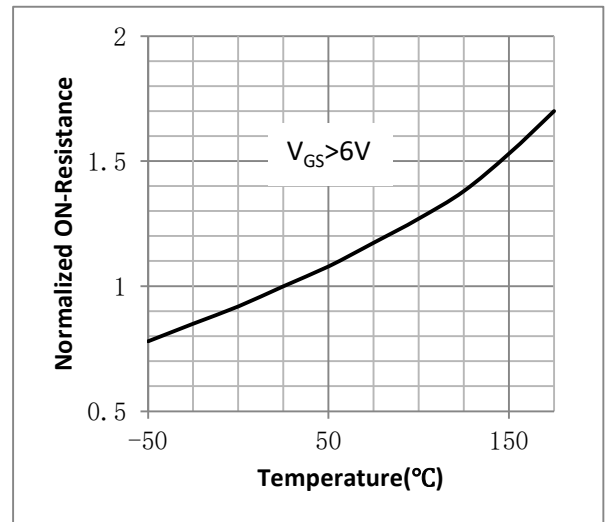


Figure 9. Diode Forward Voltage vs. Current

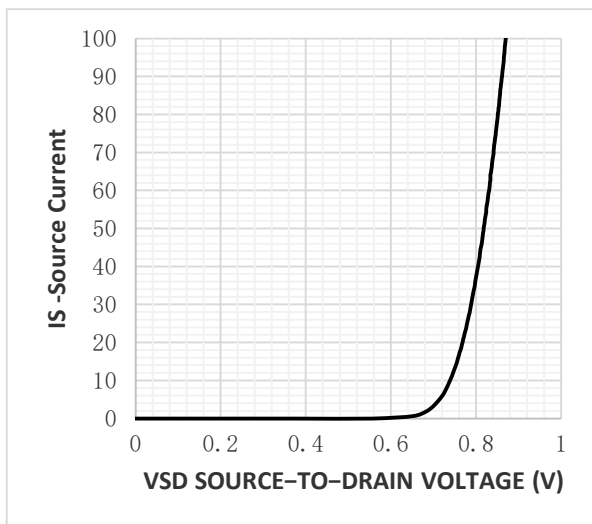


Figure 10. Transfer Characteristics

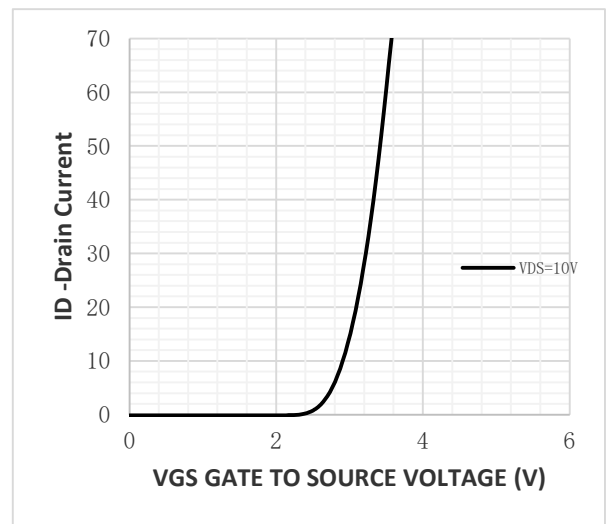
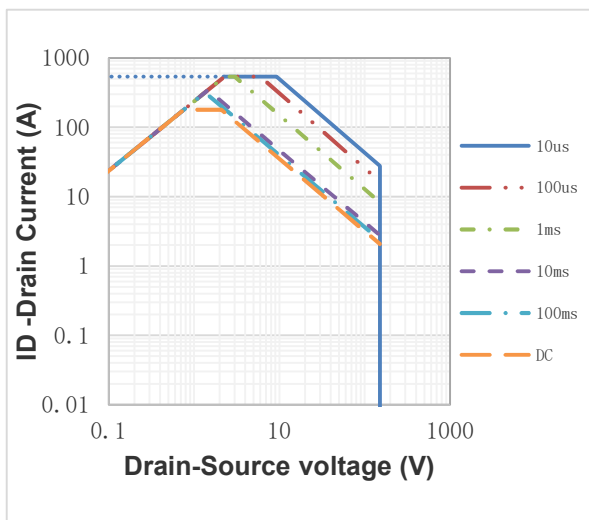
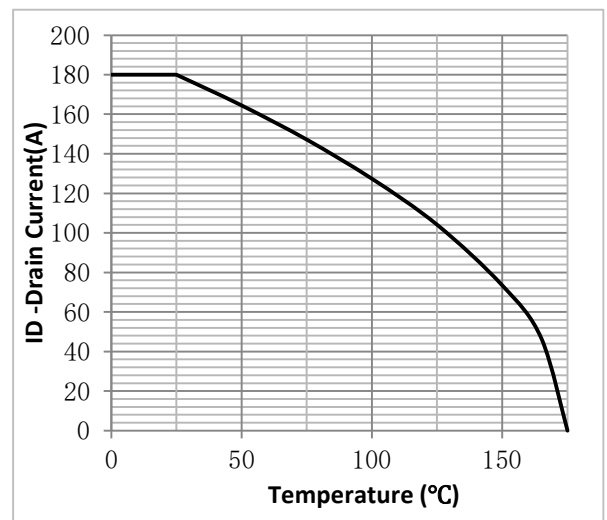
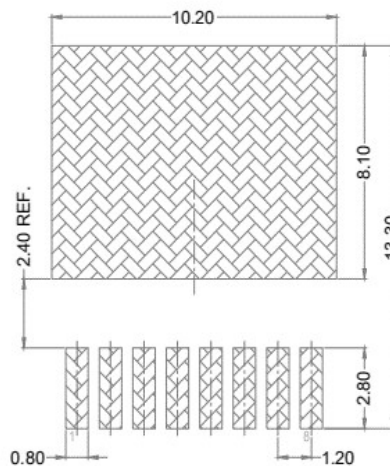
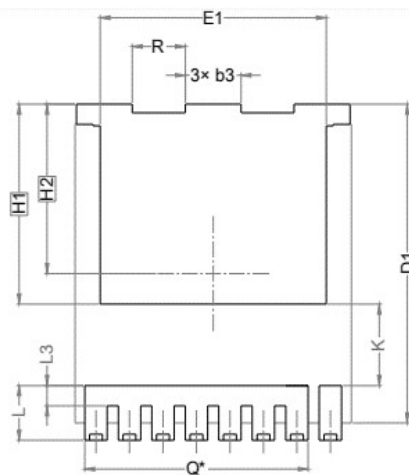
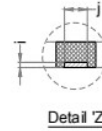
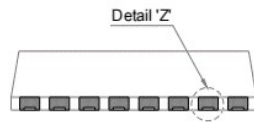
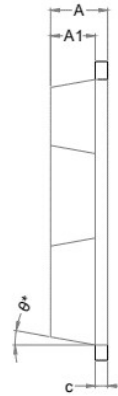
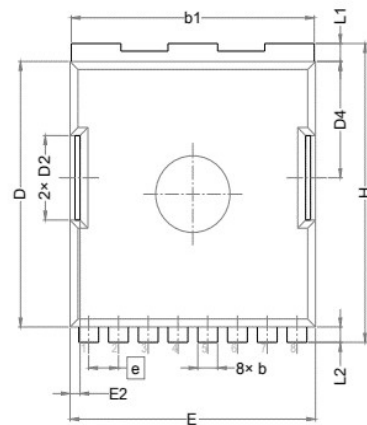


Fig.11 Safe Operating Area

Fig.12 ID vs. Junction Temperature^③



•TOLL Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.90	2.00	2.10
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
E2	0.30	0.40	0.50
e	1.20 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
H2	5.89 BSC		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.60	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.60	0.70	0.80
N	8		
Q	6.80 REF.		
R	1.80	1.90	2.00
theta	10° REF.		



Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours ;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature.
 $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2024/8/15	New